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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,617	01/10/2002	Kyu-Hyoung Cho	5000-1-237	6501
33942	7590	12/02/2004	EXAMINER	
CHA & REITER, LLC			BELLO, AGUSTIN	
210 ROUTE 4 EAST STE 103				
PARAMUS, NJ 07652			ART UNIT	PAPER NUMBER
			2633	

DATE MAILED: 12/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/043,617	CHO ET AL.	
	Examiner	Art Unit	
	Agustin Bello	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-6 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-4 and 6 is/are rejected.
 7) Claim(s) 5 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (U.S. Patent No. 5,864,416).

Regarding claim 1, Williams teaches an opto-electric converter (reference numeral 10 in Figure 1) for converting an input optical signal into an electrical signal, an amplifier circuit (reference numeral 20 in Figure 1) for amplifying the electrical signal; a bit rate-sensing circuit (inherent in reference numeral 50 in Figure 1 as described in column 3 line 67- column 4 line 5) connected to receive the amplified electrical signal for generating a sensing signal with a voltage level determined on the basis of a bit rate of the electrical signal; a bit rate-recognition circuit (inherent in reference numeral 50 in Figure 1 as described in column 3 line 67- column 4 line 5) for generating a recognition signal that is further amplified from the sensing signal, a clock/data recovery circuit (reference numeral 50 in Figure 1) for reproducing a clock signal and data from the amplified electrical signal in accordance with a control signal (reference numeral 53 in Figure 1) and outputting the reproduced clock signal and data; and, a controller (reference numeral 100 in Figure 1) for determining a bit rate corresponding to a voltage level of the recognition signal by referring to a look-up table (column 4 lines 10-12) defining a predetermined relationship of the bit rate to the voltage level, and for providing the clock/data

recovery circuit with the control signal (reference numeral 53 in Figure 1) representative of the bit rate. Williams differs from the claimed invention in that Williams fails to specifically teach that said bit rate-recognition circuit has a structure of providing an extended range of recognizable total input voltages by connecting a plurality of logarithm amplifiers in series, each of which logarithm amplifiers has a predetermined range of recognizable input voltage. However, such structures are well known in the art. Chorey, in the same field of detectors teaches such a structure (Figure 7). One skilled in the art would have been motivated to employ the structure taught by Chorey in the bit rate recognition circuit of Williams since such a structure is known to provide a dynamic range in excess of 50 dB (column 9 lines 1-3 of Chorey). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ the serial logarithm amplifier structure of Chorey in the bit rate-recognition circuit of Williams.

Regarding claim 2, the combination of references teaches a low-noise amplifier (reference numeral 20 in Figure 1 of Williams) for eliminating noise from the electrical signal outputted from the opto-electric converter (reference numeral 10 in Figure 1 of Williams) and for amplifying the noise-free electrical signal by a given amplification factor; and, a limiting amplifier (reference numeral 90 in Figure 1) for re-amplifying the amplified electrical signal within a predetermined voltage level.

Regarding claim 3, the combination of references and Chorey in particular teaches a plurality of the logarithm amplifiers connected to sequentially amplify the sensing signal outputted from the bit rate-sensing circuit (Figure 7 of Chorey); a plurality of rectifiers (reference numeral 52, 54, 56, and 58 in Figure 7 of Chorey) respectively connected to one input of the

respective logarithm amplifiers and to one output of at least one said logarithm amplifier, for rectifying the sensing signal inputted thereto; and, an adder (reference numeral 60 in Figure 1) connected to provide the sum of output signals of the plurality of rectifiers.

Regarding claim 4, the combination of references and Williams in particular teaches a phase-locked loop circuit (column 4 lines 1-2) for generating a reference clock signal in accordance with the control circuit provided by the controller (reference numeral 100 in Figure 1); and, at least one flip-flop (inherent in the clock/data recovery circuit 50 in Figure 1) connected to reproduce a clock signal (reference numeral 51 in Figure 1) and data (reference numeral 52 in Figure 1), in accordance with the reference clock signal, from the amplified electrical signal supplied from the amplifier circuit (reference numeral 95, 96 in Figure 1).

Regarding claim 6, the combination of references and Williams in particular teaches that the controller comprises a memory for storing a look-up table (column 4 lines 10-12) indicating a predetermined data set of the bit rate to the voltage level.

Allowable Subject Matter

3. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brown, Asahi, Kanesaka, Yang, and Kogure presents relevant art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Agustin Bello
Examiner
Art Unit 2633

AB

